NEC

MOS INTEGRATED CIRCUIT

# μPD42S18165, 4218165

## 16 M-BIT DYNAMIC RAM
## 1 M-WORD BY 16-BIT, EDO, BYTE READ/WRITE MODE

### Description

The μPD42S18165, 4218165 are 1,048,576 words by 16 bits CMOS dynamic RAMs with optional EDO.

EDO is a kind of the page mode and is useful for the read operation.

Besides, the μPD42S18165 can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh.

The μPD42S18165, 4218165 are packaged in 50-pin plastic TSOP (II) and 42-pin plastic SOJ.

### Features

- EDO (Hyper page mode)
- 1,048,576 words by 16 bits organization
- Single +5.0 V ± 10 % power supply
- Fast access and cycle time

| Part number | Power consumption Active (MAX.) | Access time (MAX.) | R/W cycle time (MIN.) | EDO (Hyper page mode) cycle time (MIN.) |
|---|---|---|---|---|
| μPD42S18165-50, 4218165-50 | 935 mW | 50 ns | 84 ns | 20 ns |
| μPD42S18165-60, 4218165-60 | 880 mW | 60 ns | 104 ns | 25 ns |
| μPD42S18165-70, 4218165-70 | 825 mW | 70 ns | 124 ns | 30 ns |

- *The μPD42S18165 can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh*

| Part number | Refresh cycle | Refresh | Power consumption at standby (MAX.) |
|---|---|---|---|
| μPD42S18165 | 1,024 cycles/128 ms | $\overline{CAS}$ before $\overline{RAS}$ self refresh, $\overline{CAS}$ *before* $\overline{RAS}$ *refresh*, $\overline{RAS}$ only refresh, Hidden refresh | 1.4 mW *(CMOS level input)* |
| μPD4218165 | 1,024 cycles/16 ms | $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh | 5.5 mW (CMOS level input) |



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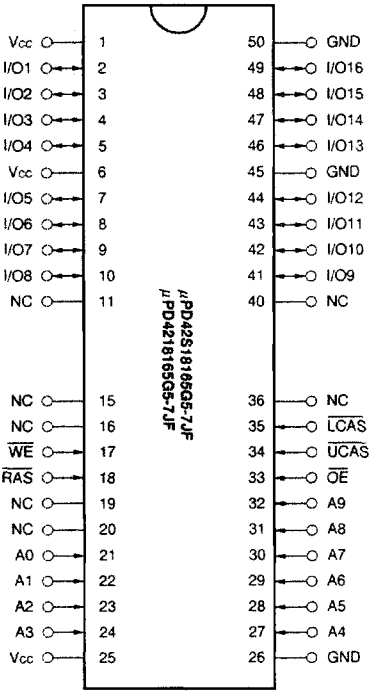
**The mark ★ shows major revised points.**

## Ordering Information

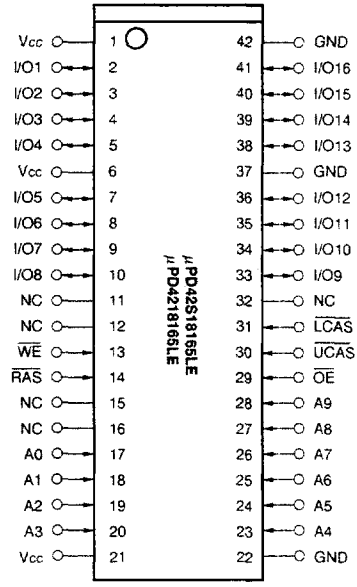
| Part number | Access time (MAX.) | Package | Refresh |
|---|---|---|---|
| μPD42S18165G5-50-7JF | 50 ns | 50-pin plastic TSOP (II) (400 mil) | $\overline{CAS}$ before $\overline{RAS}$ self refresh<br>$\overline{CAS}$ before $\overline{RAS}$ refresh<br>$\overline{RAS}$ only refresh<br>Hidden refresh |
| μPD42S18165G5-60-7JF | 60 ns | | |
| μPD42S18165G5-70-7JF | 70 ns | | |
| μPD42S18165LE-50 | 50 ns | 42-pin plastic SOJ (400 mil) | |
| μPD42S18165LE-60 | 60 ns | | |
| μPD42S18165LE-70 | 70 ns | | |
| μPD4218165G5-50-7JF | 50 ns | 50-pin plastic TSOP (II) (400 mil) | $\overline{CAS}$ before $\overline{RAS}$ refresh<br>$\overline{RAS}$ only refresh<br>Hidden refresh |
| μPD4218165G5-60-7JF | 60 ns | | |
| μPD4218165G5-70-7JF | 70 ns | | |
| μPD4218165LE-50 | 50 ns | 42-pin plastic SOJ (400 mil) | |
| μPD4218165LE-60 | 60 ns | | |
| μPD4218165LE-70 | 70 ns | | |

## Pin Configurations (Marking Side)

### 50-pin Plastic TSOP (II) (400 mil)

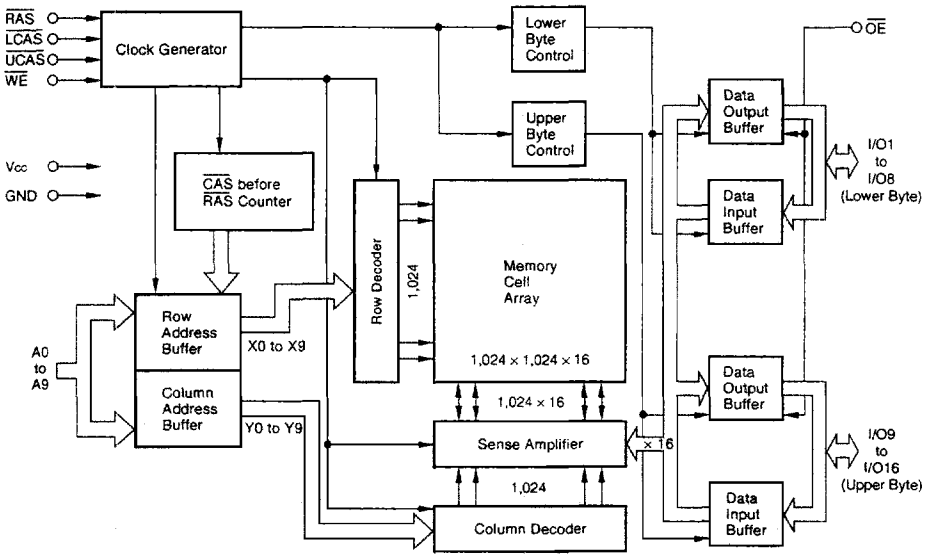



### 42-pin Plastic SOJ (400 mil)




| | | |
|---|---|---|
| A0 to A9 | : | Address Inputs |
| I/O1 to I/O16 | : | Data Inputs/Outputs |
| RAS | : | Row Address Strobe |
| UCAS | : | Column Address Strobe (upper) |
| LCAS | : | Column Address Strobe (lower) |
| WE | : | Write Enable |
| OE | : | Output Enable |
| Vcc | : | Power Supply |
| GND | : | Ground |
| NC | : | No Connection |

## Block Diagram



### Input/Output Pin Functions

The μPD42S18165, 4218165 have input pins $\overline{RAS}$, $\overline{CAS}$[Note], $\overline{WE}$, $\overline{OE}$, A0 to A9 and input/output pins I/O1 to I/O16.

| Pin name | Input/Output | Function |
|---|---|---|
| $\overline{RAS}$ (Row address strobe) | Input | $\overline{RAS}$ activates the sense amplifier by latching a row address and selecting a corresponding word line.<br>It refreshes memory cell array of one line selected by the row address.<br>It also selects the following function.<br>• $\overline{CAS}$ before $\overline{RAS}$ refresh |
| $\overline{CAS}$ (Column address strobe) | | $\overline{CAS}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier. |
| A0 to A9 (Address inputs) | | Address bus.<br>Input total 20-bit of address signal, upper 10-bit and lower 10-bit in sequence (*address multiplex method*).<br>Therefore, one word is selected from 1,048,576-word by 16-bit memory cell array.<br>In actual operation, latch row address by specifying row address and activating $\overline{RAS}$.<br>Then, switch the address bus to column address and activate $\overline{CAS}$.<br>Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated.<br>Therefore, the address input setup time ($t_{ASR}$, $t_{ASC}$) and hold time ($t_{RAH}$, $t_{CAH}$) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$. |
| $\overline{WE}$ (Write enable) | | Write control signal.<br>Write operation is executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$. |
| $\overline{OE}$ (Output enable) | | Read control signal.<br>Read operation can be executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$.<br>*If $\overline{WE}$ is activated during read operation, $\overline{OE}$ is to be ineffective in the device.*<br>Therefore, read operation cannot be executed. |
| I/O1 to I/O16 (Data inputs/outputs) | Input/Output | 16-bit data bus.<br>I/O1 to I/O16 are used to input/output data. |

**Note** $\overline{CAS}$ means $\overline{UCAS}$ and $\overline{LCAS}$.

## ★ Hyper Page Mode (EDO)

The hyper page mode (EDO) is a kind of page mode with enhanced features. The two major features of the hyper page mode (EDO) are as follows.

**1. Data output time is extended.**

In the hyper page mode (EDO), the output data is held to the next $\overline{CAS}$ cycle's falling edge, instead of the rising edge. For this reason, valid data output time in the hyper page mode (EDO) is extended compared with the fast page mode (= data extend function). In the fast page mode, the data output time becomes shorter as the $\overline{CAS}$ cycle time becomes shorter. Therefore, in the hyper page mode (EDO), the timing margin in read cycle is larger than that of the fast page mode even if the $\overline{CAS}$ cycle time becomes shorter.

**2. The $\overline{CAS}$ cycle time in the hyper page mode (EDO) is shorter than that in the fast page mode.**

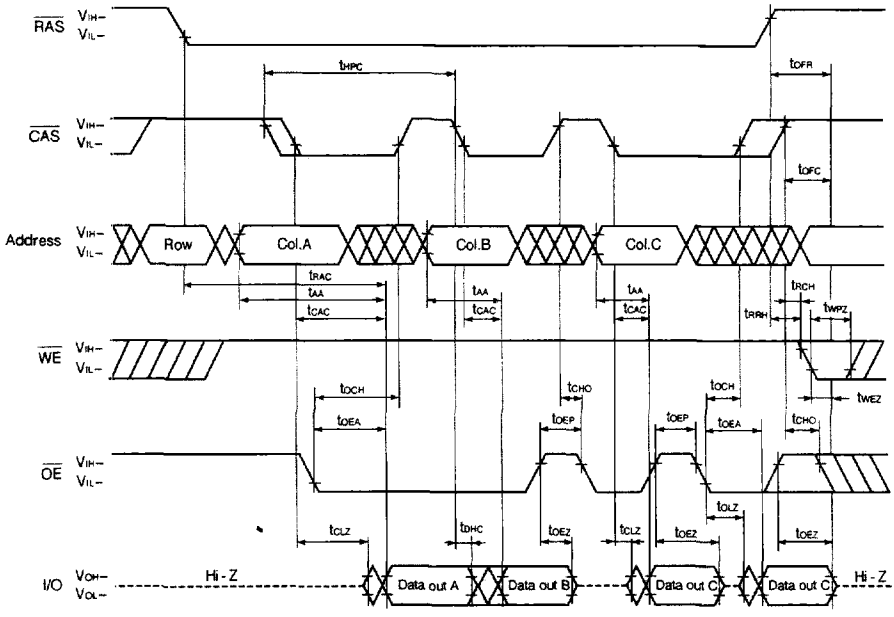
In the hyper page mode (EDO), due to the data extend function, the $\overline{CAS}$ cycle time can be shorter than in the fast page mode if the timing margin is the same.

Taking a device whose $t_{RAC}$ is 60 ns as an example, the $\overline{CAS}$ cycle time in the fast page mode is 25 ns while that in the fast page mode is 40 ns.

In the hyper page mode (EDO), read (data out) and write (data in) cycles can be executed repeatedly during one $\overline{RAS}$ cycle. The hyper page mode (EDO) allows both read and write operations during one cycle.

The following shows a part of the hyper page mode (EDO) read cycle. Specifications to be observed are described in the next page.

**Hyper Page Mode (EDO) Read Cycle**



**Cautions when using the hyper page mode (EDO)**

1. $\overline{CAS}$ access should be used to operate $t_{HPC}$ at the MIN. value.
2. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on the state of each signal.
   (1) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive (at the end of read cycle)
   $\overline{WE}$: inactive, $\overline{OE}$: active
   $t_{OFC}$ is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
   $t_{OFR}$ is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.
   The slower of $t_{OFC}$ and $t_{OFR}$ becomes effective.
   (2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)
   $\overline{WE}$, $\overline{OE}$: inactive ····· $t_{OEZ}$ is effective.
   Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive (at the end of read cycle)
   $\overline{WE}$, $\overline{OE}$: active and either $t_{RRH}$ or $t_{RCH}$ must be met ····· $t_{WEZ}$ and $t_{WPZ}$ are effective.
   The faster of $t_{OEZ}$ and $t_{WEZ}$ becomes effective.
   The faster of (1) and (2) becomes effective.
3. In read cycle, the effective specification depends on the state of $\overline{CAS}$ signal when controlling data output with the $\overline{OE}$ signal.
   (1) $\overline{CAS}$: inactive, $\overline{OE}$: active ····· $t_{CHO}$ is effective.
   (2) $\overline{CAS}$, $\overline{OE}$: active ····· $t_{OCH}$ is effective.

## Electrical Specifications

- $\overline{CAS}$ means $\overline{UCAS}$ and $\overline{LCAS}$.
- All voltages are referenced to GND.
- After power up ($V_{CC} \geq V_{CC(MIN.)}$), wait more than 100 μs ($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

### Absolute Maximum Ratings

| Parameter | Symbol | Condition | Rating | Unit |
|---|---|---|---|---|
| Voltage on any pin relative to GND | $V_T$ | | −1.0 to +7.0 | V |
| Supply voltage | $V_{CC}$ | | −1.0 to +7.0 | V |
| Output current | $I_O$ | | 50 | mA |
| Power dissipation | $P_D$ | | 1 | W |
| Operating ambient temperature | $T_A$ | | 0 to +70 | °C |
| Storage temperature | $T_{stg}$ | | −55 to +125 | °C |

**Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.**

### Recommended Operating Conditions

| Parameter | Symbol | Condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | | 4.5 | 5.0 | 5.5 | V |
| High level input voltage | $V_{IH}$ | | 2.4 | | $V_{CC}$ + 1.0 | V |
| Low level input voltage | $V_{IL}$ | | −1.0 | | +0.8 | V |
| Operating ambient temperature | $T_A$ | | 0 | | 70 | °C |

### Capacitance ($T_A$ = 25 °C, f = 1 MHz)

| Parameter | Symbol | Test condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Input capacitance | $C_{I1}$ | Address | | | 5 | pF |
| | $C_{I2}$ | $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ | | | 7 | |
| Data input/output capacitance | $C_{I/O}$ | I/O | | | 7 | pF |

**DC Characteristics (Recommended operating conditions unless otherwise noted)**

| Parameter | | Symbol | Test condition | | MIN. | MAX. | Unit | Notes |
|---|---|---|---|---|---|---|---|---|
| Operating current | | $I_{CC1}$ | $\overline{RAS}$, $\overline{CAS}$ cycling<br>$t_{RC} = t_{RC\ (MIN.)}$, $I_O$ = 0 mA | $t_{RAC}$ = 50 ns | | 170 | mA | 1, 2, 3 |
| | | | | $t_{RAC}$ = 60 ns | | 160 | | |
| | | | | $t_{RAC}$ = 70 ns | | 150 | | |
| Standby current | μPD42S18165 | $I_{CC2}$ | $\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$, $I_O$ = 0 mA | | | 2.0 | mA | |
| | | | $\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V, $I_O$ = 0 mA | | | 0.25 | | |
| | μPD4218165 | | $\overline{RAS}$, $\overline{CAS} \geq V_{IH\ (MIN.)}$, $I_O$ = 0 mA | | | 2.0 | | |
| | | | $\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V, $I_O$ = 0 mA | | | 1.0 | | |
| $\overline{RAS}$ only refresh current | | $I_{CC3}$ | $\overline{RAS}$ cycling, $\overline{CAS} \geq V_{IH\ (MIN.)}$<br>$t_{RC} = t_{RC\ (MIN.)}$, $I_O$ = 0 mA | $t_{RAC}$ = 50 ns | | 170 | mA | 1, 2, 3, 4 |
| | | | | $t_{RAC}$ = 60 ns | | 160 | | |
| | | | | $t_{RAC}$ = 70 ns | | 150 | | |
| Operating current (Hyper page mode (EDO)) | | $I_{CC4}$ | $\overline{RAS} \leq V_{IL\ (MAX.)}$, $\overline{CAS}$ cycling<br>$t_{HPC} = t_{HPC\ (MIN.)}$, $I_O$ = 0 mA | $t_{RAC}$ = 50 ns | | 120 | mA | 1, 2, 5 |
| | | | | $t_{RAC}$ = 60 ns | | 110 | | |
| | | | | $t_{RAC}$ = 70 ns | | 100 | | |
| $\overline{CAS}$ before $\overline{RAS}$ refresh current | | $I_{CC5}$ | $\overline{RAS}$ cycling<br>$t_{RC} = t_{RC\ (MIN.)}$, $I_O$ = 0 mA | $t_{RAC}$ = 50 ns | | 170 | mA | 1, 2 |
| | | | | $t_{RAC}$ = 60 ns | | 160 | | |
| | | | | $t_{RAC}$ = 70 ns | | 150 | | |
| $\overline{CAS}$ before $\overline{RAS}$ long refresh current (1,024 cycles / 128 ms, only for the μPD42S18165) | | $I_{CC6}$ | $\overline{CAS}$ before $\overline{RAS}$ refresh :<br>$t_{RC}$ = 125.0 μs<br>$\overline{RAS}$, $\overline{CAS}$:<br>$V_{CC}$ – 0.2 V ≤ $V_{IH} \leq V_{IH\ (MAX.)}$<br>0 V ≤ $V_{IL} \leq$ 0.2 V | $t_{RAS} \leq$ 300 ns | | 350 | μA | 1, 2 |
| | | | Standby:<br>$\overline{RAS}$, $\overline{CAS} \geq V_{CC}$ – 0.2 V<br>Address: $V_{IH}$ or $V_{IL}$<br>$\overline{WE}$, $\overline{OE}$: $V_{IH}$<br>$I_O$ = 0 mA | $t_{RAS} \leq$ 1 μs | | 400 | μA | 1, 2 |
| $\overline{CAS}$ before $\overline{RAS}$ self refresh current (only for the μPD42S18165) | | $I_{CC7}$ | $\overline{RAS}$, $\overline{CAS}$ :<br>$t_{RASS}$ = 5 ms<br>$V_{CC}$ – 0.2 V ≤ $V_{IH} \leq V_{IH\ (MAX.)}$<br>0 V ≤ $V_{IL} \leq$ 0.2 V<br>$I_O$ = 0 mA | | | 250 | μA | 2 |
| Input leakage current | | $I_{I(L)}$ | $V_I$ = 0 to 5.5 V<br>*All other pins not under test = 0 V* | | –10 | +10 | μA | |
| Output leakage current | | $I_{O(L)}$ | $V_O$ = 0 to 5.5 V<br>Output is disabled (Hi-Z) | | –10 | +10 | μA | |
| High level output voltage | | $V_{OH}$ | $I_O$ = –5.0 mA | | 2.4 | | V | |
| Low level output voltage | | $V_{OL}$ | $I_O$ = +4.2 mA | | | 0.4 | V | |

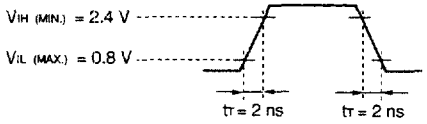
**Notes 1.** $I_{CC1}$, $I_{CC3}$, $I_{CC4}$, $I_{CC5}$ and $I_{CC6}$ depend on cycle rates ($t_{RC}$ and $t_{HPC}$).

2. Specified values are obtained with outputs unloaded.
3. $I_{CC1}$ and $I_{CC3}$ are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL\ (MAX.)}$ and $\overline{CAS} \geq V_{IH\ (MIN.)}$.
4. $I_{CC3}$ is measured assuming that all column address inputs are held at either high or low.
5. $I_{CC4}$ is measured assuming that all column address inputs are switched only once during each hyper page (EDO) cycle.

## AC Characteristics (Recommended Operating Conditions unless otherwise noted)

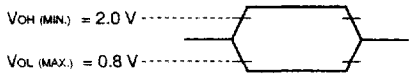
### AC Characteristics Test Conditions

(1) Input timing specification

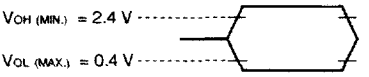



★ (2) Output timing specification

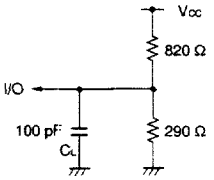
- μPD42S18165-50, 4218165-50




- μPD42S18165-60, 4218165-60
- μPD42S18165-70, 4218165-70




(3) Output loading conditions



**Common to Read, Write, Read Modify Write Cycle**

| Parameter | | Symbol | $t_{RAC}$ = 50 ns | | $t_{RAC}$ = 60 ns | | $t_{RAC}$ = 70 ns | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| Read / Write cycle time | | $t_{RC}$ | 84 | – | 104 | – | 124 | – | ns | |
| $\overline{RAS}$ precharge time | | $t_{RP}$ | 30 | – | 40 | – | 50 | – | ns | |
| ★ $\overline{CAS}$ precharge time | | $t_{CPN}$ | 8 | – | 10 | – | 10 | – | ns | |
| $\overline{RAS}$ pulse width | | $t_{RAS}$ | 50 | 10,000 | 60 | 10,000 | 70 | 10,000 | ns | 1 |
| ★ $\overline{CAS}$ pulse width | | $t_{CAS}$ | 8 | 10,000 | 10 | 10,000 | 12 | 10,000 | ns | |
| $\overline{RAS}$ hold time | | $t_{RSH}$ | 10 | – | 10 | – | 12 | – | ns | |
| $\overline{CAS}$ hold time | | $t_{CSH}$ | 38 | – | 40 | – | 50 | – | ns | |
| $\overline{RAS}$ to $\overline{CAS}$ delay time | | $t_{RCD}$ | 11 | 37 | 14 | 45 | 14 | 52 | ns | 2 |
| $\overline{RAS}$ to column address delay time | | $t_{RAD}$ | 9 | 25 | 12 | 30 | 12 | 35 | ns | 2 |
| $\overline{CAS}$ to $\overline{RAS}$ precharge time | | $t_{CRP}$ | 5 | – | 5 | – | 5 | – | ns | 3 |
| Row address setup time | | $t_{ASR}$ | 0 | – | 0 | – | 0 | – | ns | |
| Row address hold time | | $t_{RAH}$ | 7 | – | 10 | – | 10 | – | ns | |
| Column address setup time | | $t_{ASC}$ | 0 | – | 0 | – | 0 | – | ns | |
| Column address hold time | | $t_{CAH}$ | 7 | – | 10 | – | 12 | – | ns | |
| $\overline{OE}$ lead time referenced to $\overline{RAS}$ | | $t_{OES}$ | 0 | – | 0 | – | 0 | – | ns | |
| $\overline{CAS}$ to data setup time | | $t_{CLZ}$ | 0 | – | 0 | – | 0 | – | ns | |
| $\overline{OE}$ to data setup time | | $t_{OLZ}$ | 0 | – | 0 | – | 0 | – | ns | |
| $\overline{OE}$ to data delay time | | $t_{OED}$ | 10 | – | 13 | – | 15 | – | ns | |
| Masked byte write hold time referenced to $\overline{RAS}$ | | $t_{MRH}$ | 0 | – | 0 | – | 0 | – | ns | |
| Transition time (rise and fall) | | $t_T$ | 1 | 50 | 1 | 50 | 1 | 50 | ns | |
| Refresh time | μPD42S18165 | $t_{REF}$ | – | 128 | – | 128 | – | 128 | ms | 4 |
| | μPD4218165 | | – | 16 | – | 16 | – | 16 | ms | |

**Notes 1.** In $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, $t_{RAS(MAX.)}$ is 100 μs.
If 10 μs < $t_{RAS}$ < 100 μs, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh ($t_{RPS}$) is applied.

**2.** For read cycles, access time is defined as follows:

| Input conditions | Access time | Access time from $\overline{RAS}$ |
|---|---|---|
| $t_{RAD} \leq t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$ | $t_{RAC(MAX.)}$ | $t_{RAC(MAX.)}$ |
| $t_{RAD} > t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$ | $t_{AA(MAX.)}$ | $t_{RAD} + t_{AA(MAX.)}$ |
| $t_{RCD} > t_{RCD(MAX.)}$ | $t_{CAC(MAX.)}$ | $t_{RCD} + t_{CAC(MAX.)}$ |

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time ($t_{RAC}$, $t_{AA}$ or $t_{CAC}$) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD(MAX.)}$ and $t_{RCD} \geq t_{RCD(MAX.)}$ will not cause any operation problems.

**3.** $t_{CRP(MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

**4.** This specification is applied only to the μPD42S18165.

**Read Cycle**

| Parameter | Symbol | $t_{RAC}$ = 50 ns | | $t_{RAC}$ = 60 ns | | $t_{RAC}$ = 70 ns | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| Access time from $\overline{RAS}$ | $t_{RAC}$ | – | 50 | – | 60 | – | 70 | ns | 1 |
| Access time from $\overline{CAS}$ | $t_{CAC}$ | – | 13 | – | 15 | – | 18 | ns | 1 |
| Access time from column address | $t_{AA}$ | – | 25 | – | 30 | – | 35 | ns | 1 |
| Access time from $\overline{OE}$ | $t_{OEA}$ | – | 13 | – | 15 | – | 18 | ns | |
| Column address lead time referenced to $\overline{RAS}$ | $t_{RAL}$ | 25 | – | 30 | – | 35 | – | ns | |
| Read command setup time | $t_{RCS}$ | 0 | – | 0 | – | 0 | – | ns | |
| Read command hold time referenced to $\overline{RAS}$ | $t_{RRH}$ | 0 | – | 0 | – | 0 | – | ns | 2 |
| Read command hold time referenced to $\overline{CAS}$ | $t_{RCH}$ | 0 | – | 0 | – | 0 | – | ns | 2 |
| Output buffer turn-off delay time from $\overline{OE}$ | $t_{OEZ}$ | 0 | 10 | 0 | 13 | 0 | 15 | ns | 3 |
| $\overline{CAS}$ hold time to $\overline{OE}$ | $t_{CHO}$ | 5 | – | 5 | – | 5 | – | ns | 4 |

**Notes 1.** For read cycles, access time is defined as follows:

| Input conditions | Access time | Access time from $\overline{RAS}$ |
|---|---|---|
| $t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$ | $t_{RAC\ (MAX.)}$ | $t_{RAC\ (MAX.)}$ |
| $t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$ | $t_{AA\ (MAX.)}$ | $t_{RAD} + t_{AA\ (MAX.)}$ |
| $t_{RCD} > t_{RCD\ (MAX.)}$ | $t_{CAC\ (MAX.)}$ | $t_{RCD} + t_{CAC\ (MAX.)}$ |

$t_{RAD\ (MAX.)}$ and $t_{RCD\ (MAX.)}$ are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time ($t_{RAC}$, $t_{AA}$ or $t_{CAC}$) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geq t_{RAD\ (MAX.)}$ and $t_{RCD} \geq t_{RCD\ (MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ should be met in read cycles.
3. $t_{OEZ(MAX.)}$ defines the time when the output achieves the condition of Hi-Z and is not referenced to $V_{OH}$ or $V_{OL}$.
4. $\overline{WE}$: inactive (in read cycle)
   $\overline{CAS}$: inactive, $\overline{OE}$: active ····· $t_{CHO}$ is effective.
   $\overline{CAS}$, $\overline{OE}$: active ····· $t_{OCH}$ is effective.

### Write Cycle

| Parameter | Symbol | $t_{RAC}$ = 50 ns | | $t_{RAC}$ = 60 ns | | $t_{RAC}$ = 70 ns | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| $\overline{WE}$ hold time referenced to $\overline{CAS}$ | $t_{WCH}$ | 7 | – | 10 | – | 10 | – | ns | 1 |
| ★ $\overline{WE}$ pulse width | $t_{WP}$ | 8 | – | 10 | – | 10 | – | ns | 1 |
| $\overline{WE}$ lead time referenced to $\overline{RAS}$ | $t_{RWL}$ | 10 | – | 10 | – | 12 | – | ns | |
| ★ $\overline{WE}$ lead time referenced to $\overline{CAS}$ | $t_{CWL}$ | 8 | – | 10 | – | 12 | – | ns | |
| $\overline{WE}$ setup time | $t_{WCS}$ | 0 | – | 0 | – | 0 | – | ns | 2 |
| $\overline{OE}$ hold time | $t_{OEH}$ | 0 | – | 0 | – | 0 | – | ns | |
| Data-in setup time | $t_{DS}$ | 0 | – | 0 | – | 0 | – | ns | 3 |
| Data-in hold time | $t_{DH}$ | 7 | – | 10 | – | 10 | – | ns | 3 |

**Notes 1.** $t_{WP\ (MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH\ (MIN.)}$ should be met.

**2.** If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

**3.** $t_{DS\ (MIN.)}$ and $t_{DH\ (MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.

### Read Modify Write Cycle

| Parameter | Symbol | $t_{RAC}$ = 50 ns | | $t_{RAC}$ = 60 ns | | $t_{RAC}$ = 70 ns | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| Read modify write cycle time | $t_{RWC}$ | 107 | – | 133 | – | 157 | – | ns | |
| $\overline{RAS}$ to $\overline{WE}$ delay time | $t_{RWD}$ | 64 | – | 77 | – | 89 | – | ns | 1 |
| $\overline{CAS}$ to $\overline{WE}$ delay time | $t_{CWD}$ | 27 | – | 32 | – | 37 | – | ns | 1 |
| Column address to $\overline{WE}$ delay time | $t_{AWD}$ | 39 | – | 47 | – | 54 | – | ns | 1 |

**Note 1.** If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

**Hyper Page Mode (EDO)**

| | Parameter | Symbol | $t_{RAC}$ = 50 ns | | $t_{RAC}$ = 60 ns | | $t_{RAC}$ = 70 ns | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| | Read / Write cycle time | $t_{HPC}$ | 20 | – | 25 | – | 30 | – | ns | 1 |
| | $\overline{RAS}$ pulse width | $t_{RASP}$ | 50 | 125,000 | 60 | 125,000 | 70 | 125,000 | ns | |
| ★ | $\overline{CAS}$ pulse width | $t_{HCAS}$ | 8 | 10,000 | 10 | 10,000 | 12 | 10,000 | ns | |
| ★ | $\overline{CAS}$ precharge time | $t_{CP}$ | 8 | – | 10 | – | 10 | – | ns | |
| | Access time from $\overline{CAS}$ precharge | $t_{ACP}$ | – | 30 | – | 35 | – | 40 | ns | |
| | $\overline{CAS}$ precharge to $\overline{WE}$ delay time | $t_{CPWD}$ | 41 | – | 52 | – | 59 | – | ns | 2 |
| | $\overline{RAS}$ hold time from $\overline{CAS}$ precharge | $t_{RHCP}$ | 30 | – | 35 | – | 40 | – | ns | |
| | Read modify write cycle time | $t_{HPRWC}$ | 52 | – | 66 | – | 75 | – | ns | |
| | Data output hold time | $t_{DHC}$ | 5 | – | 5 | – | 5 | – | ns | |
| | $\overline{OE}$ to $\overline{CAS}$ hold time | $t_{OCH}$ | 5 | – | 5 | – | 5 | – | ns | 3 |
| | $\overline{OE}$ precharge time | $t_{OEP}$ | 5 | – | 5 | – | 5 | – | ns | |
| | Output buffer turn-off delay from $\overline{WE}$ | $t_{WEZ}$ | 0 | 10 | 0 | 13 | 0 | 15 | ns | 4, 5 |
| ★ | $\overline{WE}$ pulse width | $t_{WPZ}$ | 8 | – | 10 | – | 10 | – | ns | 5 |
| | Output buffer turn-off delay from $\overline{RAS}$ | $t_{OFR}$ | 0 | 10 | 0 | 13 | 0 | 15 | ns | 4, 5 |
| | Output buffer turn-off delay from $\overline{CAS}$ | $t_{OFC}$ | 0 | 10 | 0 | 13 | 0 | 15 | ns | 4, 5 |

**Notes 1.** $t_{HPC\ (MIN.)}$ is applied to $\overline{CAS}$ access.

**2.** If $t_{WCS} \geq t_{WCS\ (MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD\ (MIN.)}$, $t_{CWD} \geq t_{CWD\ (MIN.)}$, $t_{AWD} \geq t_{AWD\ (MIN.)}$ and $t_{CPWD} \geq t_{CPWD\ (MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

**3.** $\overline{WE}$: inactive (in read cycle)
$\overline{CAS}$: inactive, $\overline{OE}$: active ····· $t_{CHO}$ is effective.
$\overline{CAS}$, $\overline{OE}$: active ····· $t_{OCH}$ is effective.

**4.** $t_{OFC\ (MAX.)}$, $t_{OFR\ (MAX.)}$ and $t_{WEZ\ (MAX.)}$ define the time when the output achieves the conditions of Hi-Z and is not referenced to $V_{OH}$ or $V_{OL}$.

**5.** To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on state of each signal.

(1) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive (at the end of the read cycle)
$\overline{WE}$: inactive, $\overline{OE}$: active
$t_{OFC}$ is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
$t_{OFR}$ is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.
The slower of $t_{OFC}$ and $t_{OFR}$ becomes effective.

(2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)
$\overline{WE}$, $\overline{OE}$: inactive ····· $t_{OEZ}$ is effective.
Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive (at the end of read cycle)
$\overline{WE}$, $\overline{OE}$: active and either $t_{RRH}$ or $t_{RCH}$ must be met ····· $t_{WEZ}$ and $t_{WPZ}$ are effective.
The faster of $t_{OEZ}$ and $t_{WEZ}$ becomes effective.

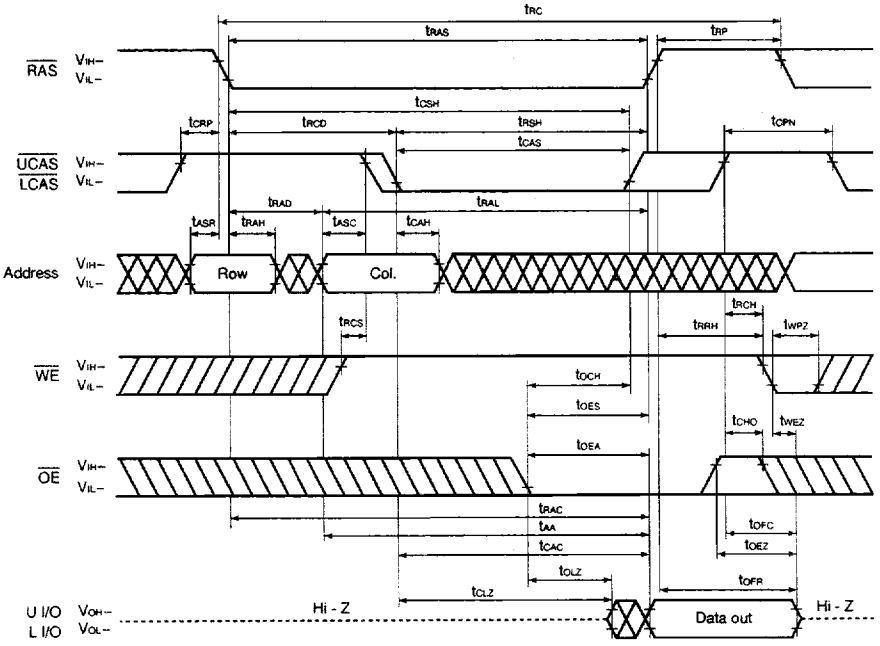
The faster of (1) and (2) becomes effective.

**Refresh Cycle**

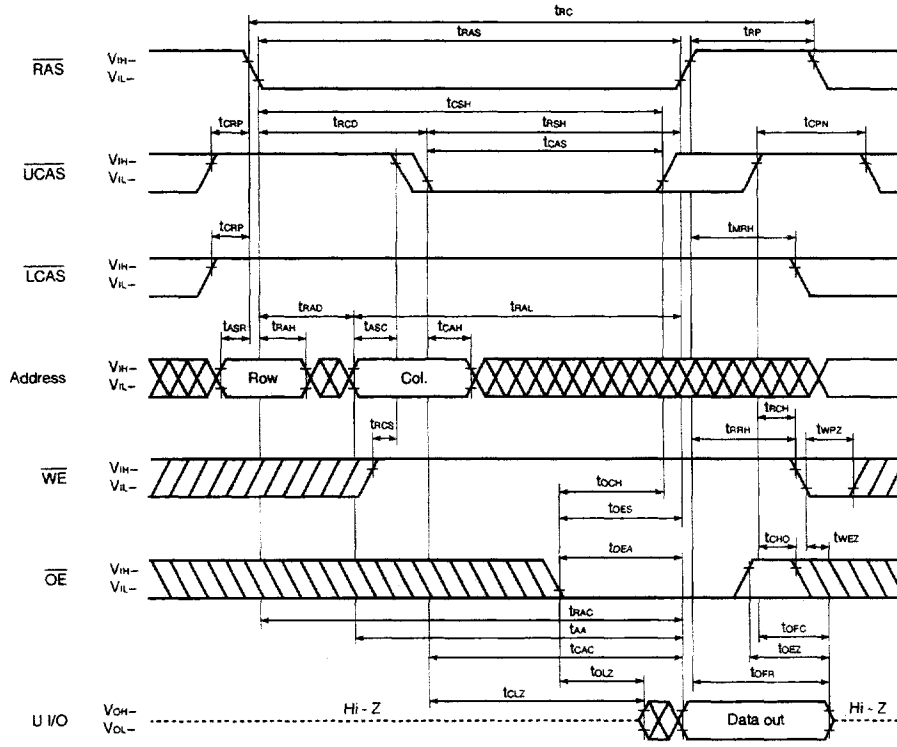
| Parameter | Symbol | $t_{RAC}$ = 50 ns | | $t_{RAC}$ = 60 ns | | $t_{RAC}$ = 70 ns | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| $\overline{CAS}$ setup time | $t_{CSR}$ | 5 | – | 5 | – | 5 | – | ns | |
| $\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ refresh) | $t_{CHR}$ | 10 | – | 10 | – | 10 | – | ns | |
| $\overline{RAS}$ precharge $\overline{CAS}$ hold time | $t_{RPC}$ | 5 | – | 5 | – | 5 | – | ns | |
| $\overline{RAS}$ pulse width ($\overline{CAS}$ before $\overline{RAS}$ self refresh) | $t_{RASS}$ | 100 | – | 100 | – | 100 | – | μs | 1 |
| $\overline{RAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$ self refresh) | $t_{RPS}$ | 90 | – | 110 | – | 130 | – | ns | 1 |
| $\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ self refresh) | $t_{CHS}$ | –50 | – | –50 | – | –50 | – | ns | 1 |
| $\overline{WE}$ hold time | $t_{WHR}$ | 15 | – | 15 | – | 15 | – | ns | |

**Note 1.** This specification is applied only to the μPD42S18165.

**Read Cycle**

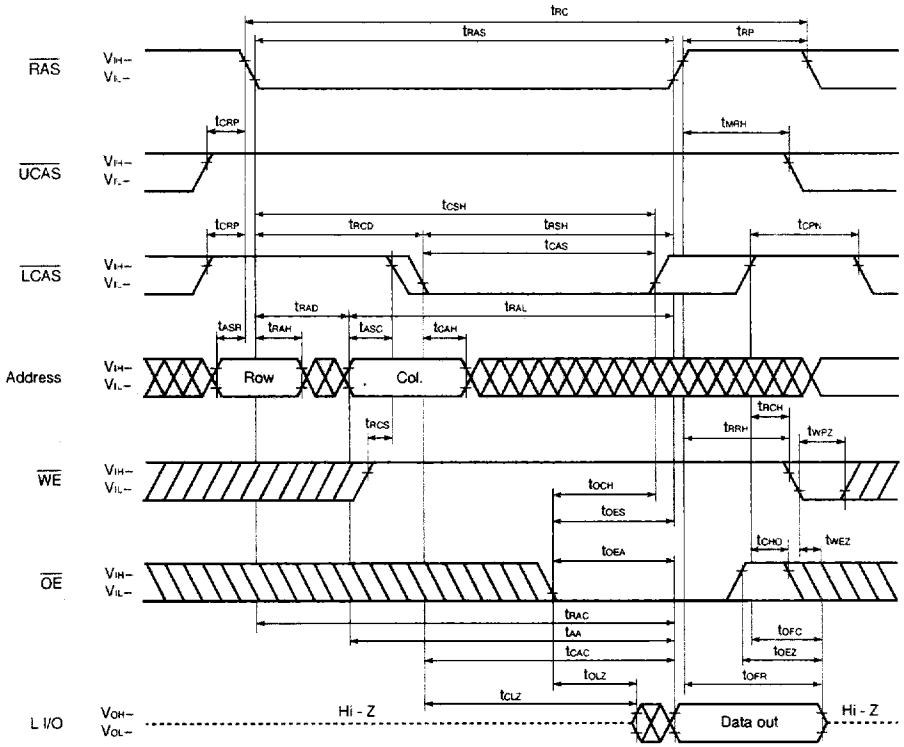

tRC
tRAS
tRP
RAS VIH– VIL–
tCSH
tCRP
tRCD
tRSH
tCAS
tOPN
UCAS VIH– LCAS VIL–
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address VIH– VIL–
Row
Col.
tRCS
tRCH
tRRH
tWPZ
WE VIH– VIL–
tOCH
tOES
tCHO
tWEZ
tOEA
OE VIH– VIL–
tRAC
tAA
tOFC
tCAC
tOEZ
tOLZ
tOFR
tCLZ
U I/O VOH– L I/O VOL–
Hi - Z
Data out
Hi - Z

**Upper Byte Read Cycle**



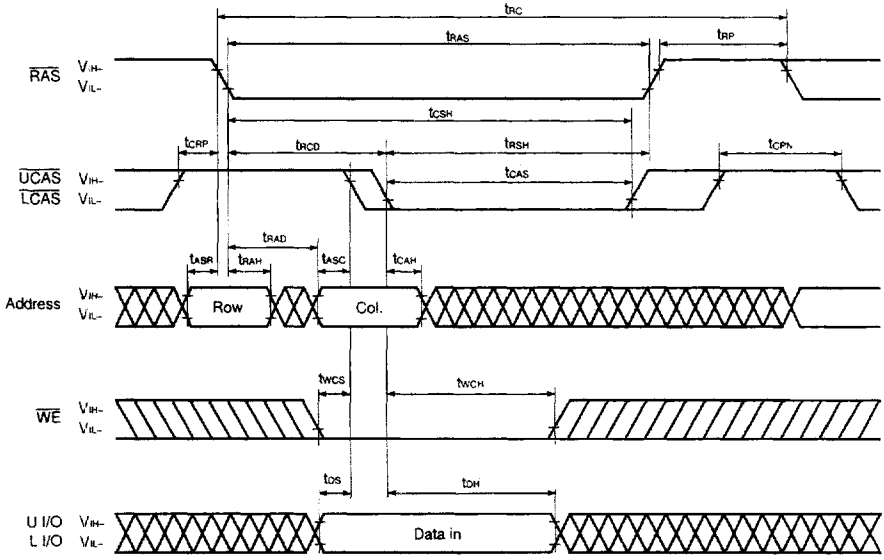

**Remark** L I/O: Hi-Z

**Lower Byte Read Cycle**



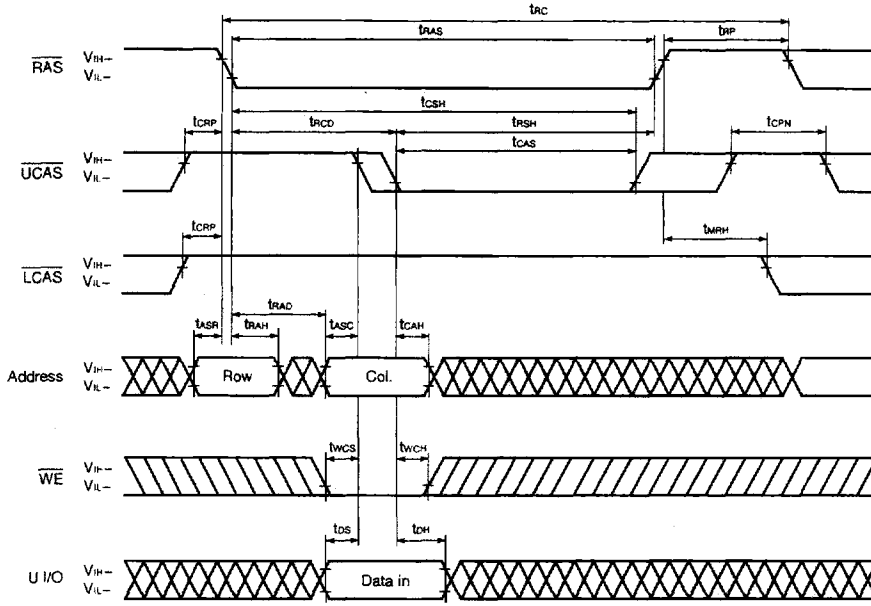

**Remark** U I/O: Hi-Z

**Early Write Cycle**



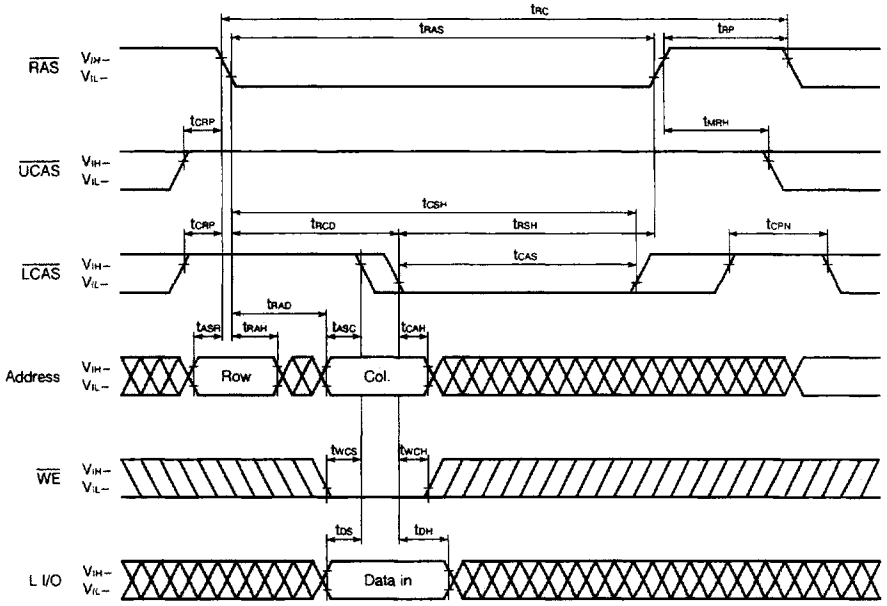

**Remark** $\overline{OE}$: Don't care

**Upper Byte Early Write Cycle**



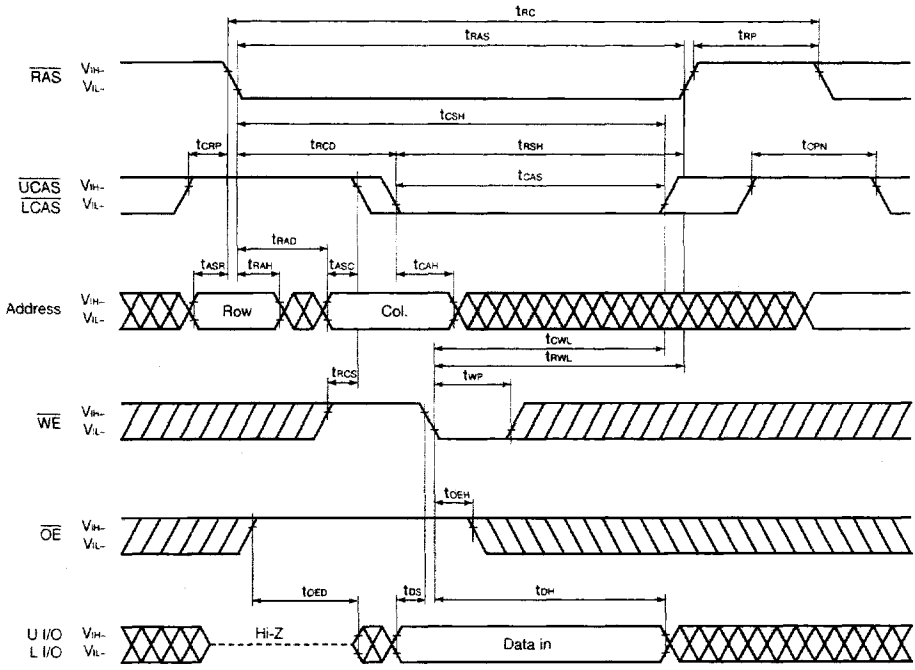

**Remark** $\overline{OE}$, L I/O: Don't care

**Lower Byte Early Write Cycle**

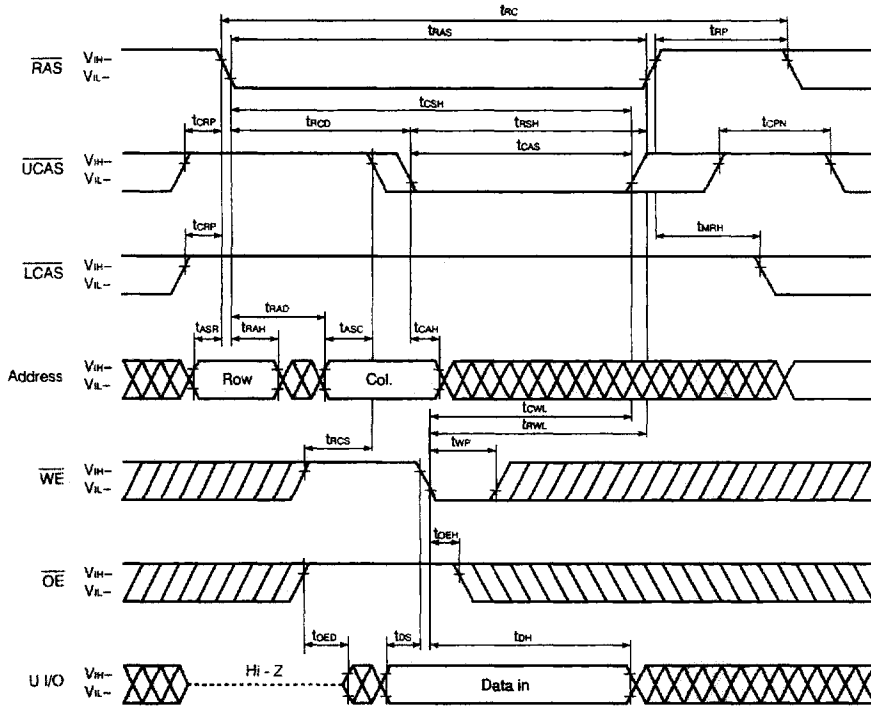



**Remark** $\overline{OE}$, U I/O: Don't care

**Late Write Cycle**

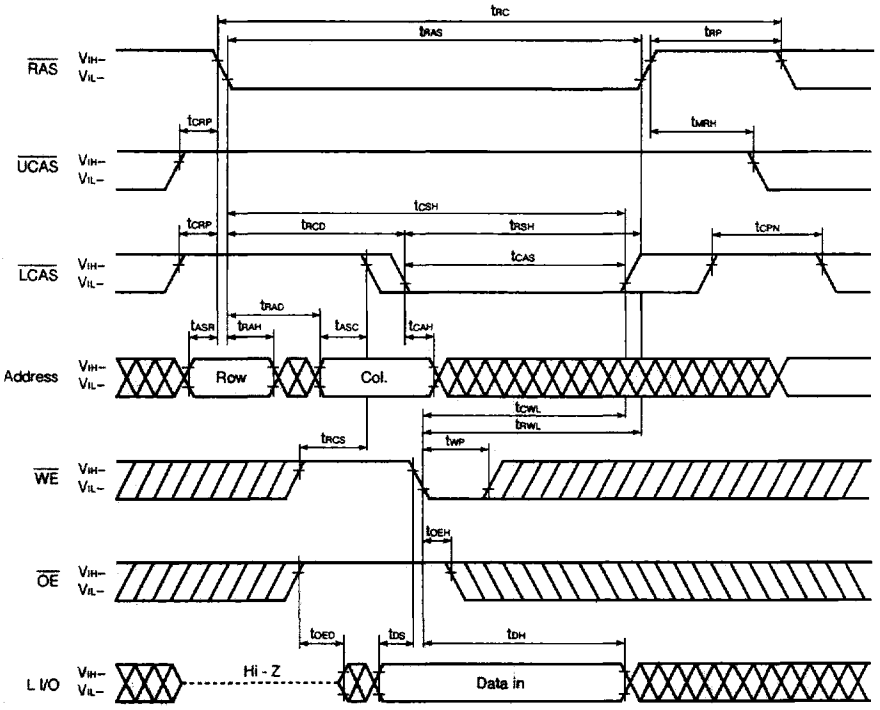


**Upper Byte Late Write Cycle**



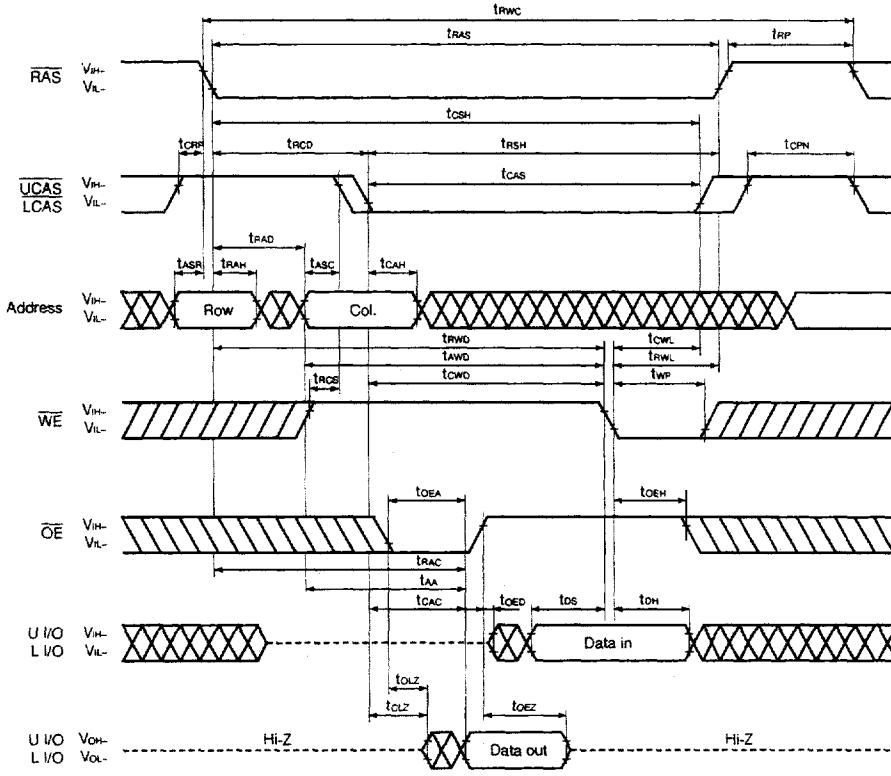

**Remark** L I/O: Don't care

**Lower Byte Late Write Cycle**

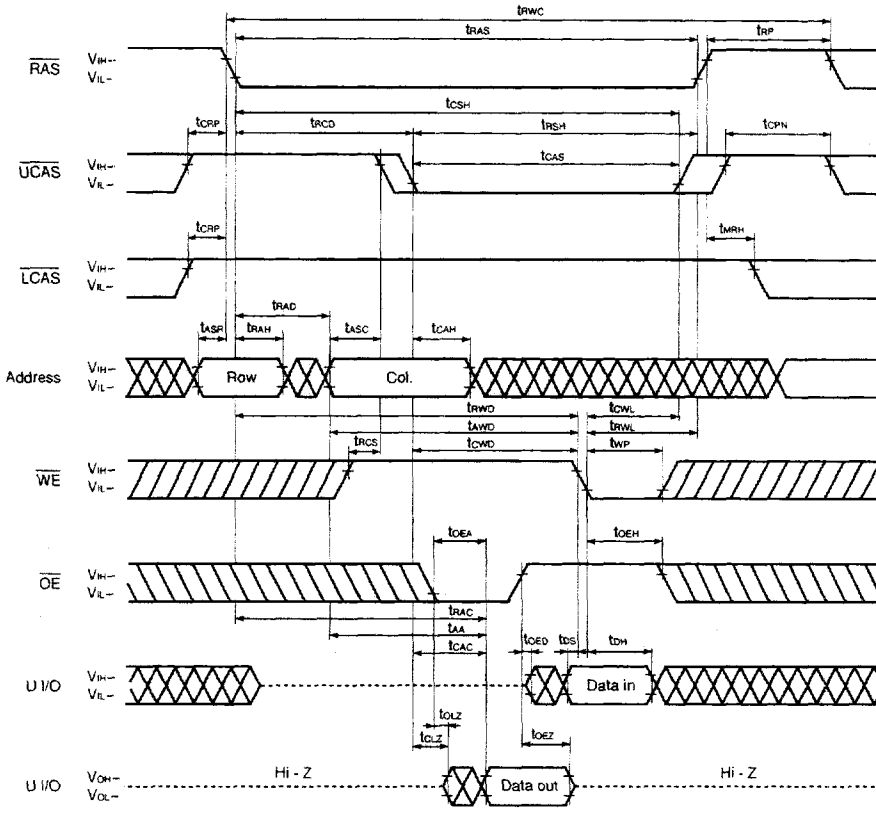



**Remark** U I/O: Don't care

**Read Modify Write Cycle**

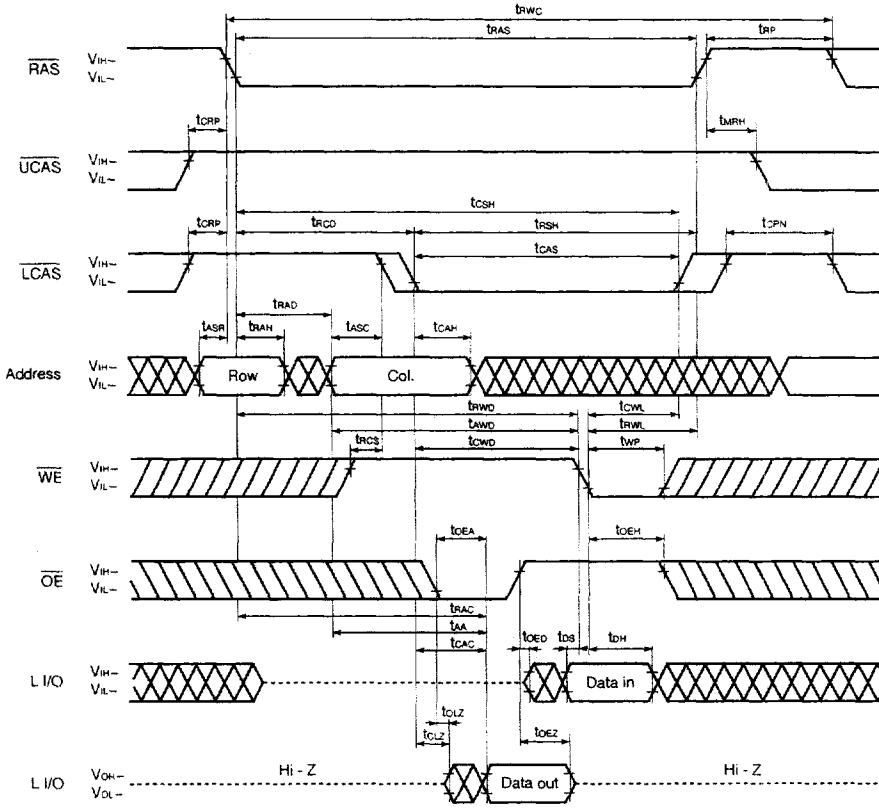


**Upper Byte Read Modify Write Cycle**



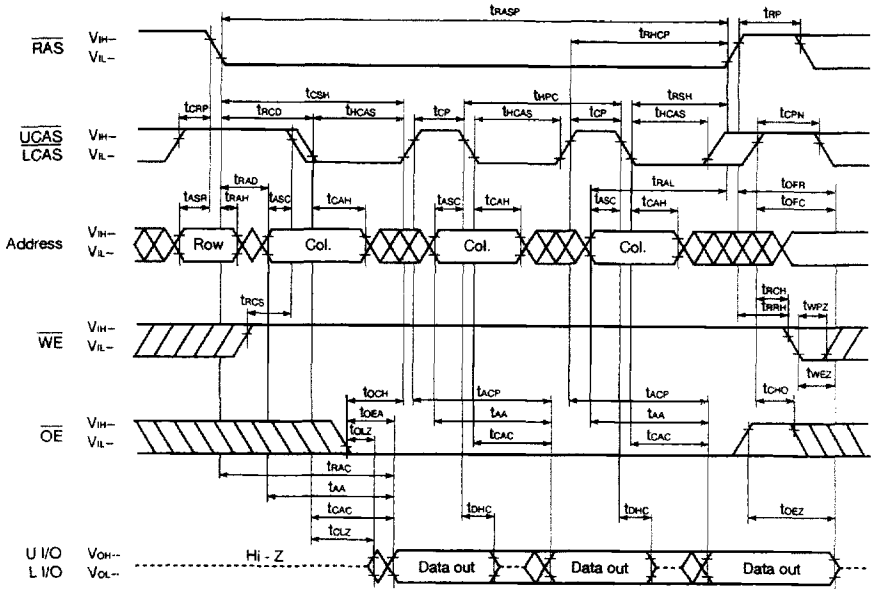

**Remark** In this cycle, the input data to Lower I/O is ineffective. The data out of that remains Hi-Z.

**Lower Byte Read Modify Write Cycle**



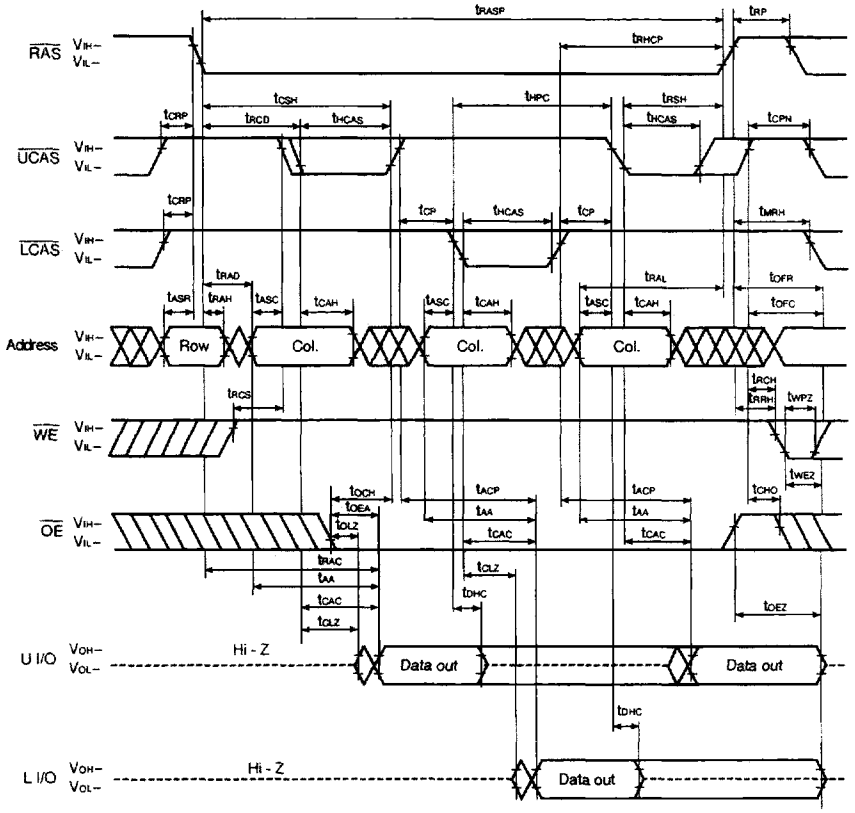

**Remark** In this cycle, the input data to Upper I/O is ineffective. The data out of that remains Hi-Z.

**Hyper Page Mode (EDO) Read Cycle**




**Remark** In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

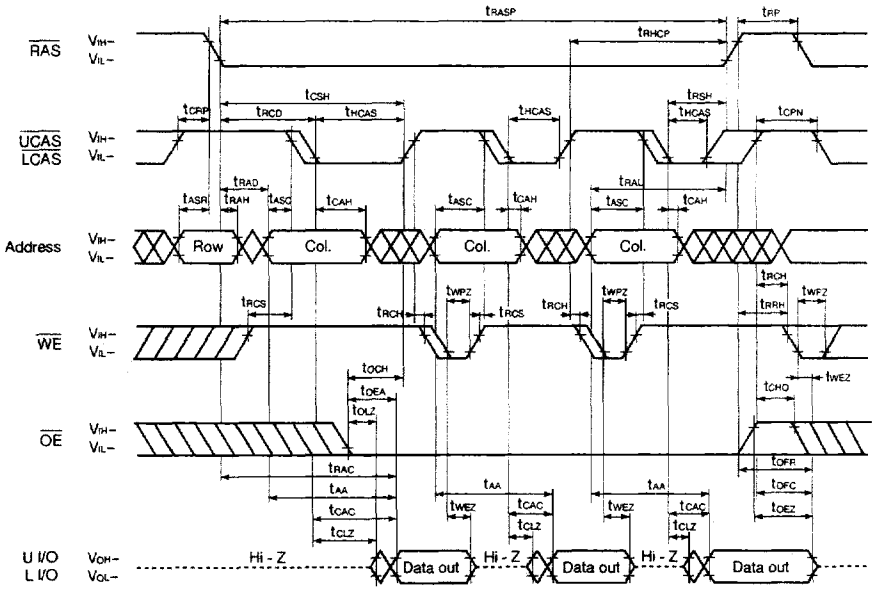
**Hyper Page Mode (EDO) Byte Read Cycle**




**Remark** 1. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

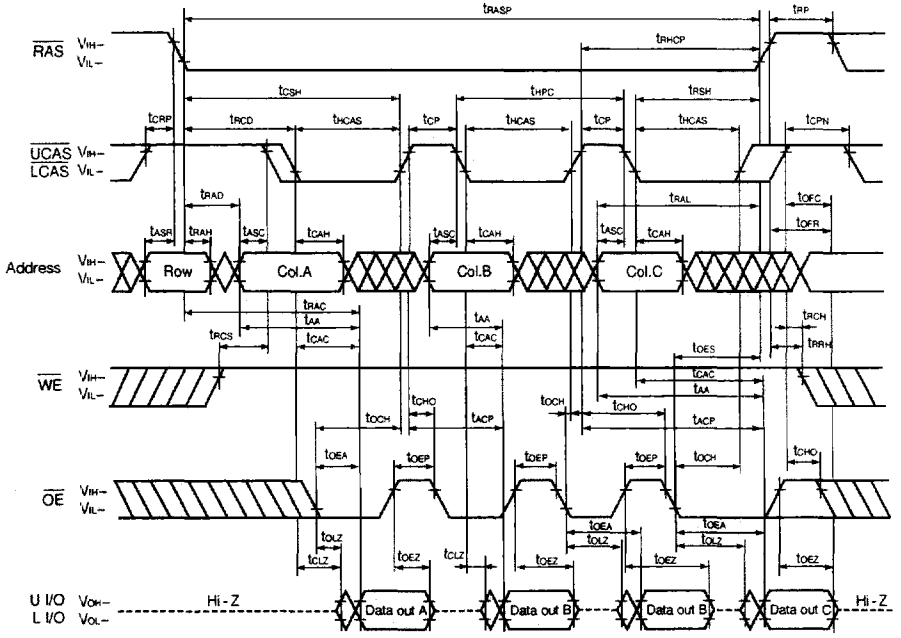
2. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

**Hyper Page Mode (EDO) Read Cycle ($\overline{WE}$ Control)**



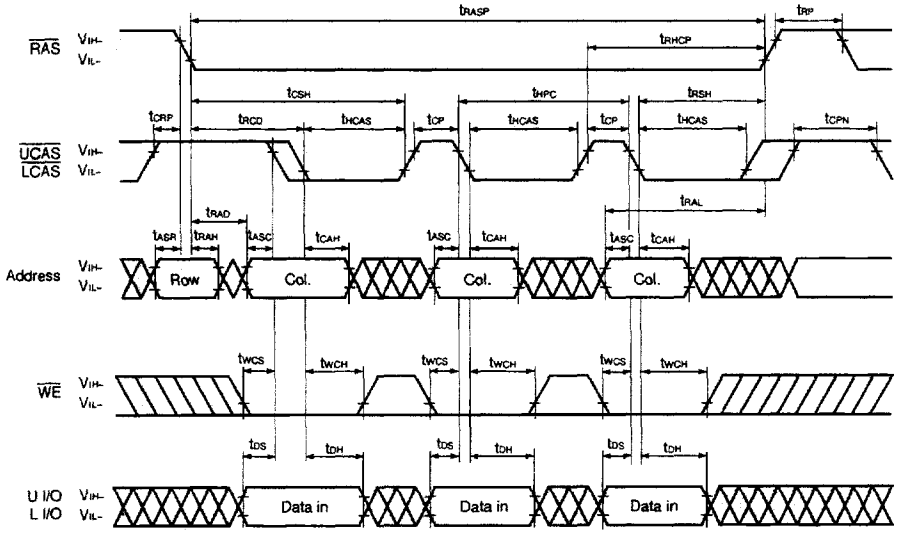

**Remark** In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

**Hyper Page Mode (EDO) Read Cycle ($\overline{OE}$ Control)**




**Remark** In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

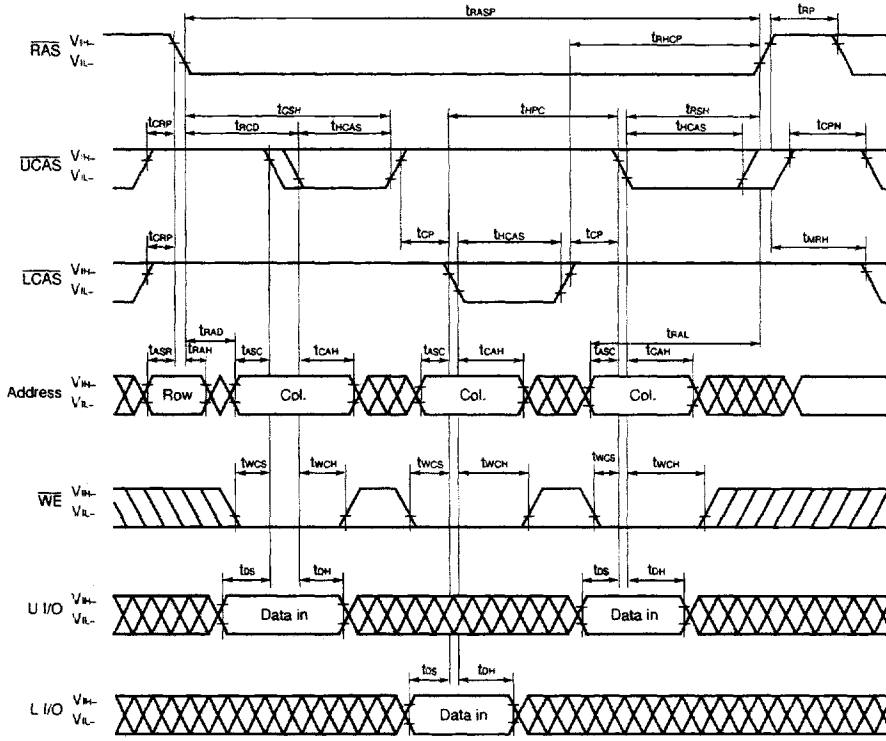
**Hyper Page Mode (EDO) Early Write Cycle**




**Remarks 1.** $\overline{OE}$: Don't care

**2.** In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

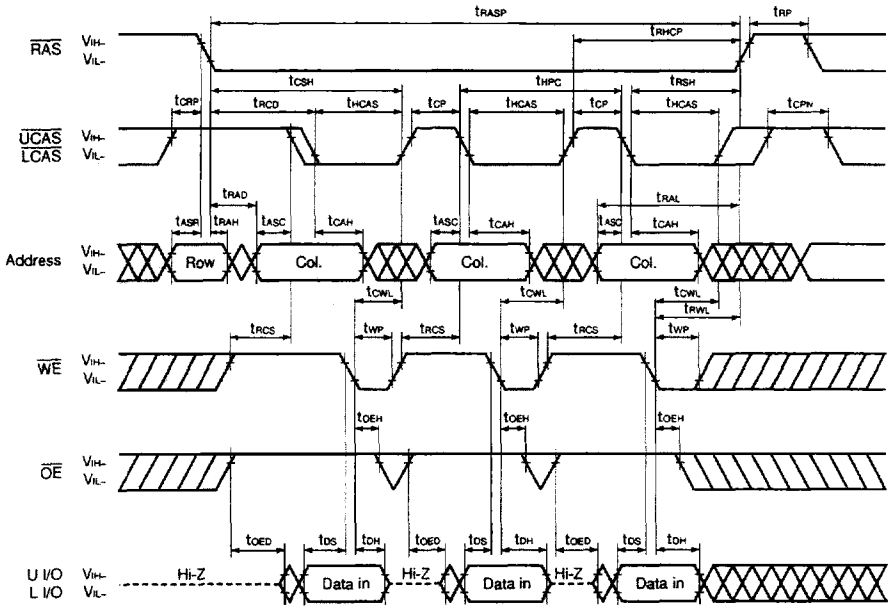
**Hyper Page Mode (EDO) Byte Early Write Cycle**




**Remarks 1.** $\overline{OE}$: Don't care

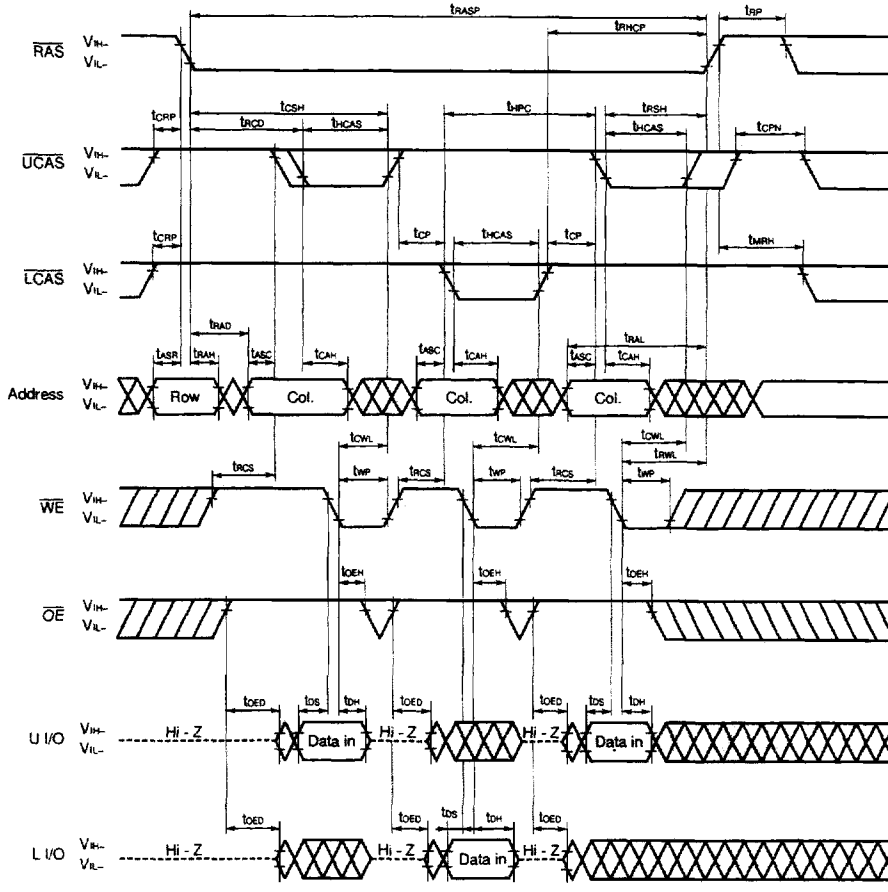
2. In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.
3. This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

**Hyper Page Mode (EDO) Late Write Cycle**




**Remark** In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

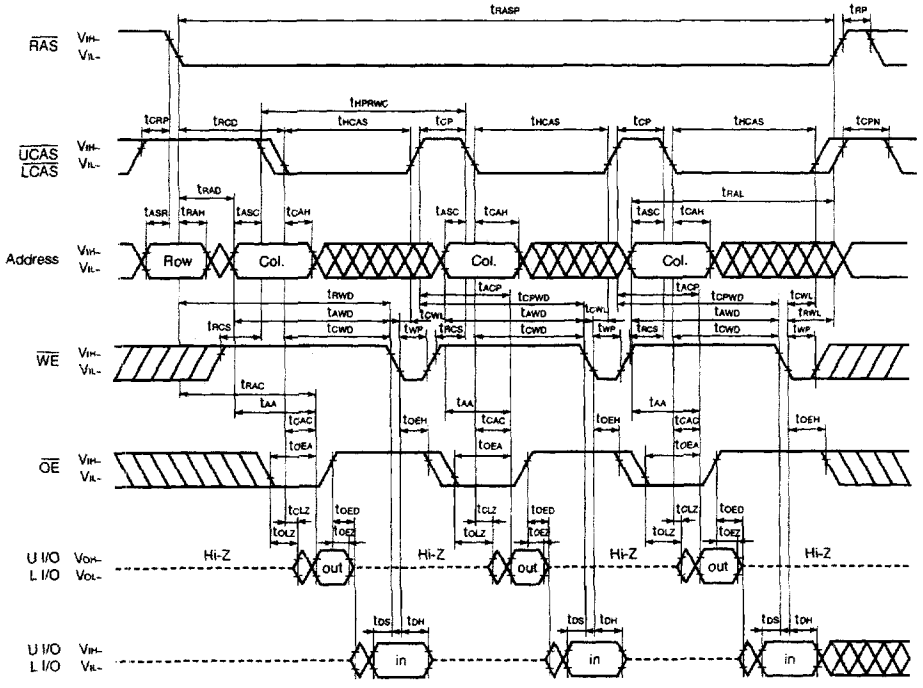
**Hyper Page Mode (EDO) Byte Late Write Cycle**




**Remarks 1.** In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

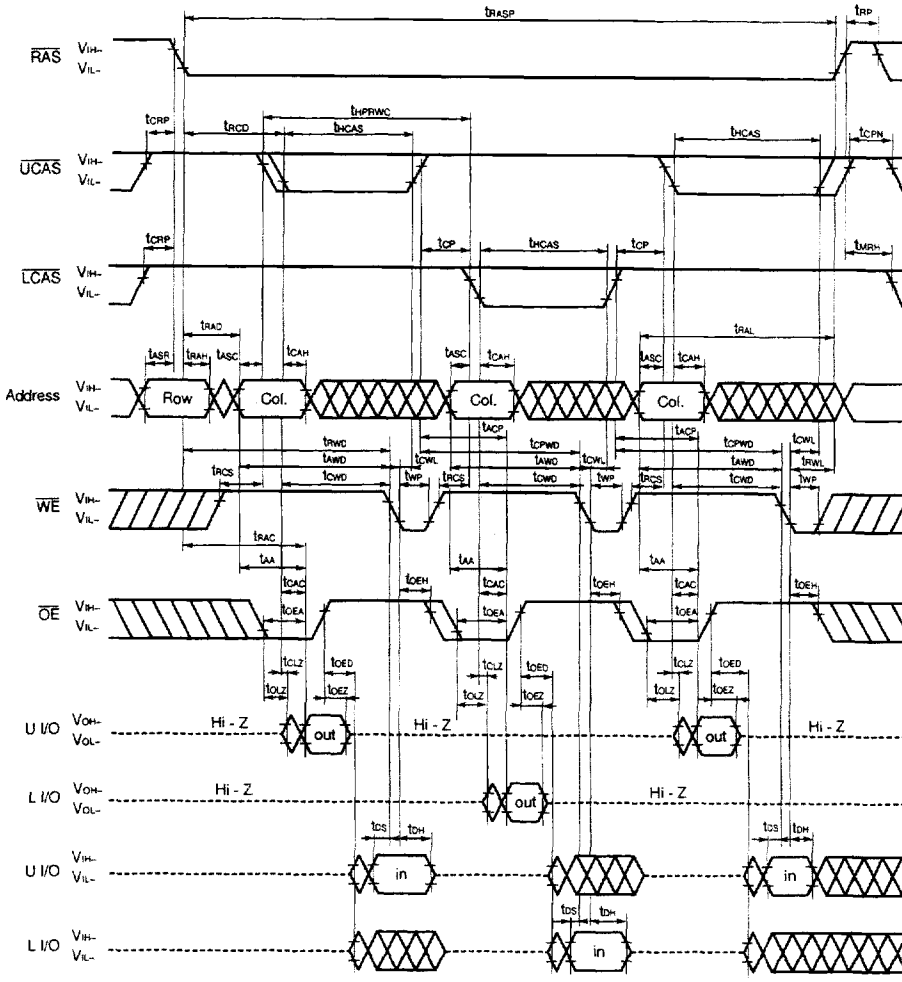
**2.** This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

**Hyper Page Mode (EDO) Read Modify Write Cycle**




**Remark** In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

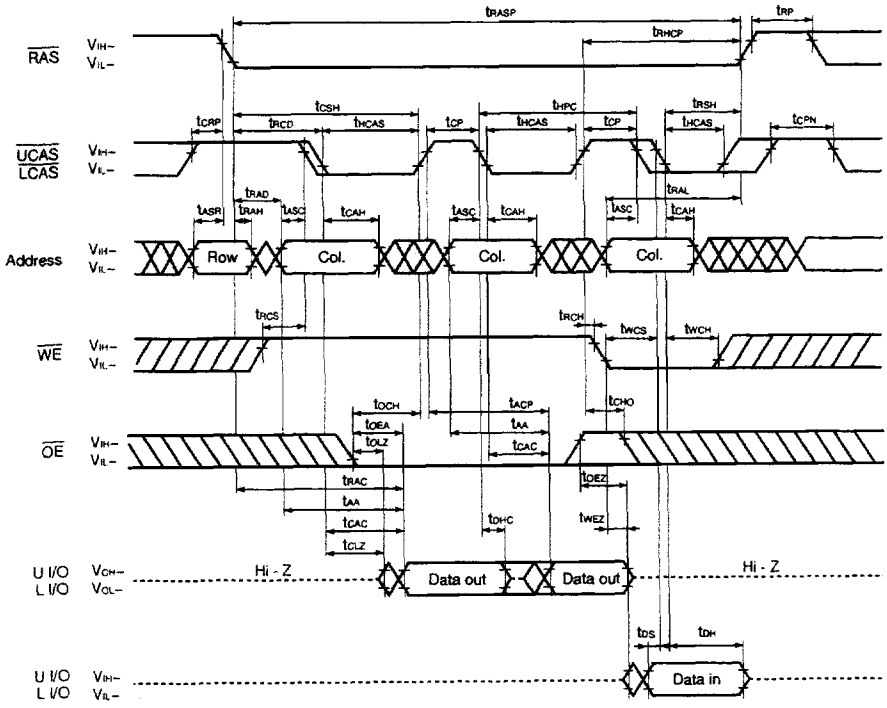
**Hyper Page Mode (EDO) Byte Read Modify Write Cycle**




**Remarks 1.** In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

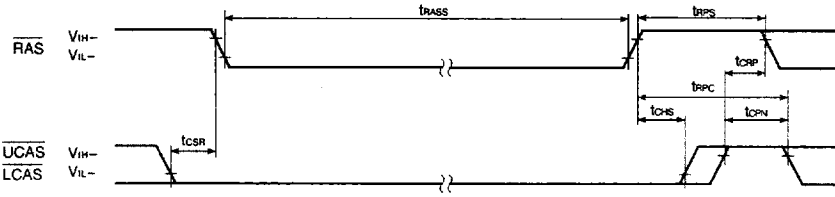
**2.** This cycle can be used to control either $\overline{UCAS}$ or $\overline{LCAS}$ only. Or, it can be used to control $\overline{UCAS}$ or $\overline{LCAS}$ simultaneously, or at random.

**Hyper Page Mode (EDO) Read and Write Cycle**




**Remark** In the hyper page mode (EDO), read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

**$\overline{CAS}$ Before $\overline{RAS}$ Self Refresh Cycle (Only for the μPD42S18165)**




**Remark** Address, $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

**Cautions on Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh**

$\overline{CAS}$ before $\overline{RAS}$ self refresh can be used independently when used in combination with distributed $\overline{CAS}$ before $\overline{RAS}$ long refresh; However, when used in combination with burst $\overline{CAS}$ before $\overline{RAS}$ long refresh or with long $\overline{RAS}$ only refresh (both distributed and burst), the following cautions must be observed.

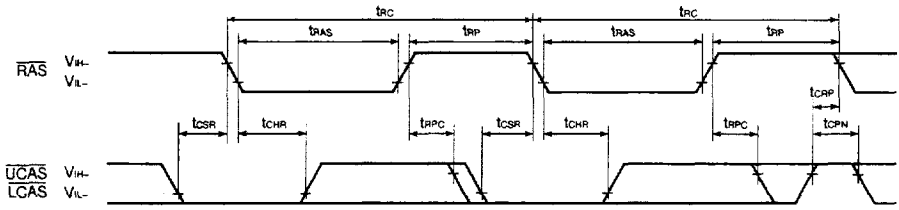
**(1) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Burst $\overline{CAS}$ Before $\overline{RAS}$ Long Refresh**
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and burst $\overline{CAS}$ before $\overline{RAS}$ long refresh are used in combination, please perform $\overline{CAS}$ before $\overline{RAS}$ refresh 1,024 times within a 16 ms interval just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

**(2) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Long $\overline{RAS}$ Only Refresh**
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and $\overline{RAS}$ only refresh are used in combination, please perform $\overline{RAS}$ only refresh 1,024 times within a 16 ms interval just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

**(3)** If $t_{RASS(MIN.)}$ is not satisfied at the beginning of $\overline{CAS}$ before $\overline{RAS}$ self refresh cycles ($t_{RAS} < 100$ μs), $\overline{CAS}$ before $\overline{RAS}$ refresh cycles will be executed one time.
If 10 μs < $t_{RAS}$ < 100 μs, $\overline{RAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ self refresh ($t_{RPS}$) is applied.
And refresh cycles (1,024/128 ms) should be met.

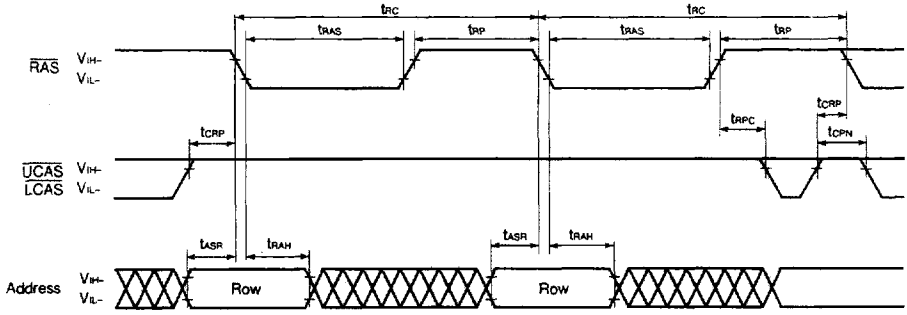
For details, please refer to **How to use DRAM** User's Manual.

### $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



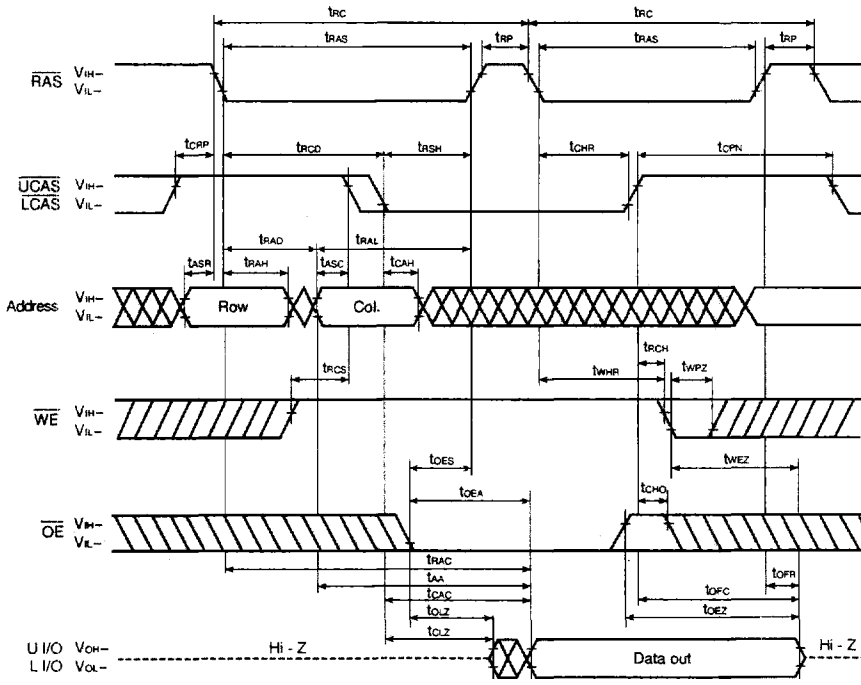

**Remark** Address, $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

### $\overline{RAS}$ Only Refresh Cycle

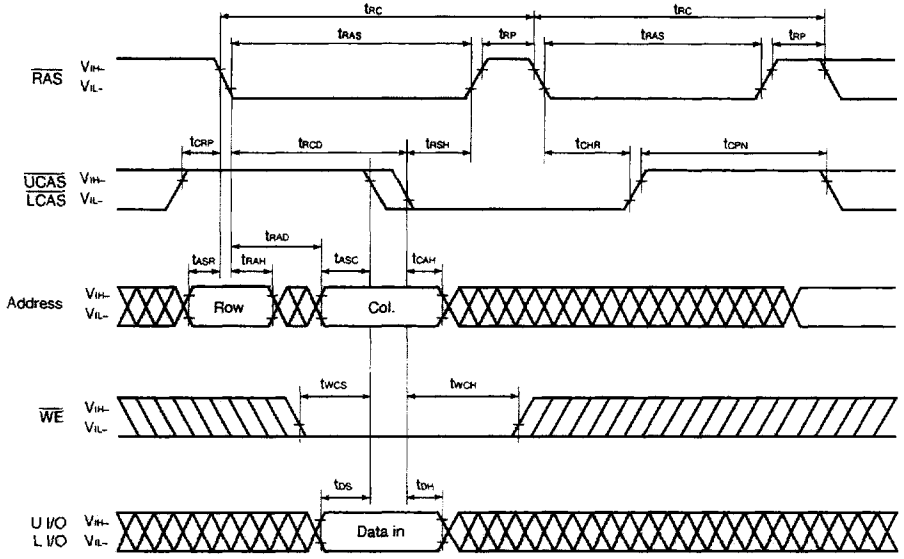



**Remark** $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O: Hi-Z

**Hidden Refresh Cycle (Read)**



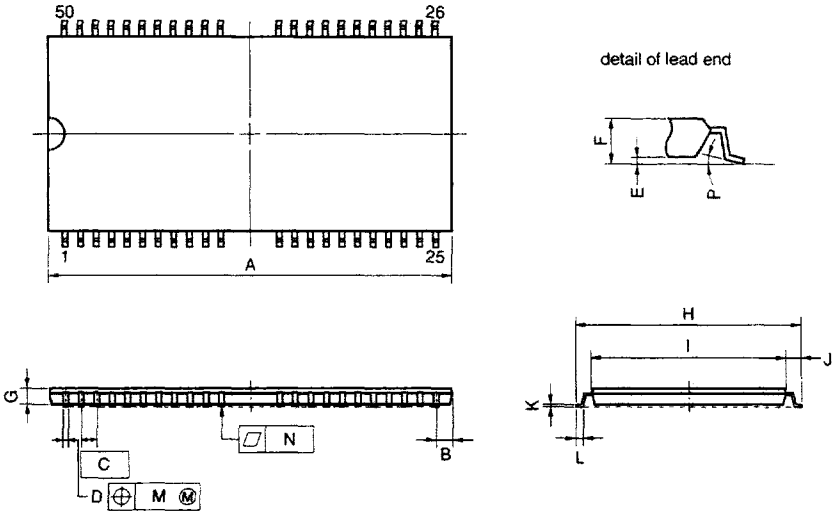
**Hidden Refresh Cycle (Write)**




**Remark** $\overline{OE}$: Don't care

*Package Drawings*

## 50PIN PLASTIC TSOP(II) (400 mil)



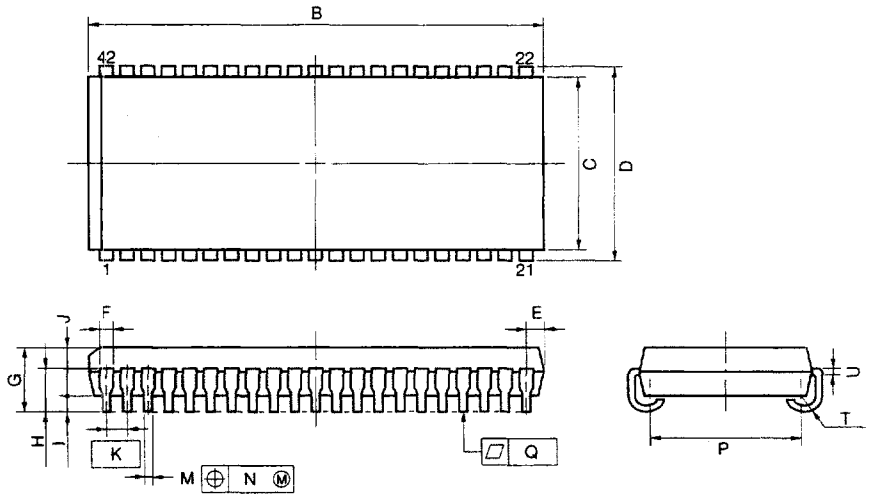

**NOTE**

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS | INCHES |
|---|---|---|
| A | 21.17 MAX. | 0.834 MAX. |
| B | 1.0 MAX. | 0.040 MAX. |
| C | 0.8 (T.P.) | 0.031 (T.P.) |
| D | $0.32^{+0.08}_{-0.07}$ | 0.013±0.003 |
| E | 0.1±0.05 | 0.004±0.002 |
| F | 1.2 MAX. | 0.048 MAX. |
| G | 0.97 | 0.038 |
| H | 11.76±0.2 | 0.463±0.008 |
| I | 10.16±0.1 | 0.400±0.004 |
| J | 0.8±0.2 | $0.031^{+0.009}_{-0.008}$ |
| K | $0.145^{+0.025}_{-0.015}$ | 0.006±0.001 |
| L | 0.5±0.1 | $0.020^{+0.004}_{-0.005}$ |
| M | 0.13 | 0.005 |
| N | 0.10 | 0.004 |
| P | $3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$ | $3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$ |

S50G5-80-7JF4

**42 PIN PLASTIC SOJ (400 mil)**




P42LE-400A

**NOTE**

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS | INCHES |
|---|---|---|
| B | $27.56^{+0.2}_{-0.35}$ | $1.085^{+0.008}_{-0.014}$ |
| C | 10.16 | 0.400 |
| D | 11.18±0.2 | 0.440±0.008 |
| E | 1.08±0.15 | $0.043^{+0.006}_{-0.007}$ |
| F | 0.74 | 0.029 |
| G | 3.5±0.2 | 0.138±0.008 |
| H | 2.545±0.2 | 0.100±0.008 |
| I | 0.8 MIN. | 0.031 MIN. |
| J | 2.6 | 0.102 |
| K | 1.27 (T.P.) | 0.050 (T.P.) |
| M | 0.40±0.10 | $0.016^{+0.004}_{-0.005}$ |
| N | 0.12 | 0.005 |
| P | 9.4±0.20 | 0.370±0.008 |
| Q | 0.10 | 0.004 |
| T | R 0.85 | R 0.033 |
| U | $0.20^{+0.10}_{-0.05}$ | $0.008^{+0.004}_{-0.002}$ |

★ **Recommended Soldering Conditions**

The following conditions (see tables below and next page) must be met for soldering conditions of the μPD42S18165, 4218165.

For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E).

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

### Types of Surface Mount Device

**μPD42S18165G5-7JF, 4218165G5-7JF: 50-pin plastic TSOP (II) (400 mil)**

| Soldering process | Soldering conditions | Symbol |
|---|---|---|
| Infrared ray reflow | Peak temperature of package surface: 235 °C or lower,<br>Reflow time: 30 seconds or less (210 °C or higher),<br>Number of reflow processes: MAX. 3<br>Exposure limit: 7 days[Note]<br>(10 hours pre-baking is required at 125 °C afterwards) | IR35-107-3 |
| VPS | Peak temperature of package: 215 °C or lower,<br>Reflow time: 40 seconds or less (200 °C or higher),<br>Number of reflow processes: MAX. 3<br>Exposure limit: 7 days[Note]<br>(10 hours pre-baking is required at 125 °C afterwards) | VP15-107-3 |
| Partial heating method | Terminal temperature: 300 °C or lower,<br>Time: 3 seconds or lower (Per side of the package). | – |

**Note** Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

**Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".**

**μPD42S18165LE, 4218165LE: 42-pin plastic SOJ (400 mil)**

| Soldering process | Soldering conditions | Symbol |
|---|---|---|
| Infrared ray reflow | Peak temperature of package surface: 235 °C or lower,<br>Reflow time: 30 seconds or less (210 °C or higher),<br>Number of reflow processes: MAX. 3<br>Exposure limit: 7 days[Note]<br>(20 hours pre-baking is required at 125 °C afterwards) | IR35-207-3 |
| VPS | Peak temperature of package: 215 °C or lower,<br>Reflow time: 40 seconds or less (200 °C or higher),<br>Number of reflow processes: MAX. 3<br>Exposure limit: 7 days[Note]<br>(20 hours pre-baking is required at 125 °C afterwards) | VP15-207-3 |
| Partial heating method | Terminal temperature: 300 °C or lower,<br>Time: 3 seconds or less (Per side of the package). | – |

**Note** Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

**Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".**